

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	34	(spill and (register block code)) same ((load and store) with instruction\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 08:10
S2	10	(spill same (parallel and (register instruction architecture pipeline))) and ((load and store) with instruction\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 15:53
S3	17	(spill same ("load/store" (load and store) with instruction\$2)) and (parallel and (register instruction architecture pipeline))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 15:55
S4	117166	(storing loading writ\$3 rewritten (memory near5 allocat\$3)) with ((register spill\$2) or (register near4 (spill and (code instruction)) ))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 15:59
S5	4	S4 and ((parallel allocator) same register) and (generat\$4 near4 (spill near2 instruction))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 16:00
S6	10	S4 and ((allocator) same register) and ((spill near2 instruction))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 16:00
S7	35	S4 and spill.clm. and ((load and store) with instruction\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 16:01
S8	2	@rlad<"20030703" and S4 and (spill and register).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 16:06

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S9	1	load\$3 near5 (register adj2 spill) adj6 (pipeline parallel)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 14:57
S10	2	"5574933".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/31 16:49
S11	7	(reus\$3 reallocat\$4 reload\$4) near5 ((STSPILL)(spill adj2 (instruction code)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 14:42
S12	748	(move store load) near3 ((multiple parallel list) near2 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:00
S13	3	S12 and spill and (register near allocat\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 14:44
S14	6	((allocation spill load) near3 ((multiple) near2 register)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 14:57
S17	29	((allocation spill load) same ((multiple) near2 register)).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 14:57
S22	12	((register same allocat\$3)) and S17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 14:59

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S23	12	S22 and ((multiple parallel list) near2 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:00
S24	12	S23 and ((multiple) near2 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:04
S25	0	S24 and ((overflow spill) same register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:02
S26	9	(concurrent near2 (move load store)) and ((overflow spill) same register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:02
S27	19	(spill and overflow) and ((multiple) near2 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:06
S28	71	reload\$4 same ((multiple) near2 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:06
S30	18	spill and ((reload\$4 move store) with ((multiple concurrent) with register))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:07
S31	3	(S12 S17 S28) and S30	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/01 15:08

## EAST Search History

S32	9	(register same (allocat\$3 resource) same spill) and (((multiple bank) near4 register) same (load store))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 10:36
S33	19	(register near4 bank with parallel) and (register with (allocat\$4 spill))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 10:41
S34	12	(register near4 bank with parallel) with (simultaneous\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 10:45
S35	0	S34 and spill	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:16
S36	140	(double near2 (load reload store)) and (register with (allocat\$4 spill))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:17
S37	109	S36 and (register adj2 (bank file))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:18
S38	62	S37 and ((double-word)(double adj word)) and ((parallel simultaneous\$3) with (store load copy))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:19
S39	0	S38 and (register with spill with reload\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:20

## EAST Search History

S40	0	S38 and (register with spill same reload\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:20
S41	0	S38 and (spill same reload\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:20
S42	54	S38 and ((register stack) same reload\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:22
S43	0	S42 and (spill with register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:21
S44	0	S42 and (spill same register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:21
S45	0	S42 and (spill)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:21
S46	54	S42 and parallel and (register with allocat\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:22
S47	0	S46 not Silverbrook	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:23

## EAST Search History

S48	8	S38 not S42	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:23
S49	16	(US-20040148490-\$ or US-20030200422-\$ or US-20050132307-\$).did. or (US-6009272-\$ or US-5530866-\$ or US-4571678-\$ or US-5574933-\$ or US-7086045-\$ or US-7007271-\$ or US-7127592-\$ or US-5867684-\$ or US-6665793-\$ or US-5946491-\$ or US-6314513-\$ or US-4980819-\$ or US-4530052-\$).did.	US-PGPUB; USPAT	OR	OFF	2007/02/02 11:34
S50	1	S49 and spill and (double near4 (load store reload word))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:37
S51	1	S49 and (multiple adj2 (register instruction)) and spill	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:38
S52	4	S49 and (multiple adj2 (register instruction))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:39
S53	3	S52 and ((register with (bank file overflow)) spill)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:56
S54	9	S49 and (register same spill)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 11:57

## EAST Search History

S55	3	S54 and (( restor\$4 rewrite reload\$3) same multiple)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:07
S56	2	S49 and (one near clock near cycle)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:11
S57	9	MOVEM same (move near3 multiple)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:14
S58	19	(double adj word) and (load near4 multiple with register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:17
S59	428	(double adj word) same ( (pair two multiple) with register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:17
S60	46	(register with allocat\$4 spill) and ((double adj word) with ( (pair two multiple) with register))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:19
S61	3	S60 and spill	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:22
S62	0	S49 and multi-register and spill	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:22

## EAST Search History

S63	1	S49 and multi-register and allocat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/02 13:22
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**Web**Results 1 - 10 of about **74,600** for **double word reload spill instructions**. (0.15 seconds)**Roger Sayle - [Committed] PR17236: Improve double-word multiply ...**

Unfortunately, **reload** and the i386 backend still conspire against us, ... Perform a **double word** multiplication of + operands OP0 and OP1 both of mode MODE, ...  
[gcc.gnu.org/ml/gcc-patches/2005-03/msg01386.html](http://gcc.gnu.org/ml/gcc-patches/2005-03/msg01386.html) - 25k - [Cached](#) - [Similar pages](#)

**RegisterAllocation - GCC Wiki**

But in the end, **reload** may decide differently, and it sometimes makes stupid choices ... For instance, moving a **double word** register one register at a time. ...  
[gcc.gnu.org/wiki/RegisterAllocation](http://gcc.gnu.org/wiki/RegisterAllocation) - 24k - [Cached](#) - [Similar pages](#)

**[PDF] The Named-State Register File: implementation and performanc ...**

File Format: PDF/Adobe Acrobat

less **spill** and **reload** traffic to switch between concurrent. contexts. The NSF speeds execution of ... 10% as many registers as an NSF with **double word** lines ...  
[ieeexplore.ieee.org/iel2/3040/8763/00386560.pdf?arnumber=386560](http://ieeexplore.ieee.org/iel2/3040/8763/00386560.pdf?arnumber=386560) - [Similar pages](#)

**[PDF] The store-load address table and speculative register promotion ...**

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**s p i l l**. and. **reload**. These are store and load **instructions** with special opcodes ... In other **words**, there is a pointer that might point to something the ...  
[ieeexplore.ieee.org/iel5/7216/19431/00898074.pdf](http://ieeexplore.ieee.org/iel5/7216/19431/00898074.pdf) - [Similar pages](#)

**[PDF] The Named-State Register File: Implementation and Performance**

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context switches generates high register **spill** and **reload**. traffic. ... 10% as many registers as an NSF with **double word** lines ...  
[doi.ieeeecomputersociety.org/10.1109/HPCA.1995.386560](http://doi.ieeeecomputersociety.org/10.1109/HPCA.1995.386560) - [Similar pages](#)

**Synergistic Processing in Cell's Multicore Architecture**

The register file can provide a single quadword element, two 64-bit **double-word** elements, four 32-bit **word** elements, eight 16-bit halfword elements, ...  
[doi.ieeeecomputersociety.org/10.1109/MM.2006.41](http://doi.ieeeecomputersociety.org/10.1109/MM.2006.41) - [Similar pages](#)

**[PS] The Store-Load Address Table and Speculative Register Promotion ...**

File Format: Adobe PostScript

**spill** and **reload**. These are store and load **instructions** with special opcodes to ... These numbers **double**-count any overlap that occurs because a variable ...  
[portal.acm.org/ft\\_gateway.cfm?id=360152&type=ps](http://portal.acm.org/ft_gateway.cfm?id=360152&type=ps) - [Similar pages](#)

**[PDF] 29K Family Simulators Reference Manual**File Format: PDF/Adobe Acrobat - [View as HTML](#)

**instruction** bus utilization, data bus utilization, register **spill**/fill histogram, ... allocated 32 Kbytes (the default allocation) on a **double word** boundary ...  
[www.amd.com/epd/29k/sims\\_man/sims\\_man.pdf](http://www.amd.com/epd/29k/sims_man/sims_man.pdf) - [Similar pages](#)

**[PDF] A Framework for End-to-End Evaluation of Register Allocators**File Format: PDF/Adobe Acrobat - [View as HTML](#)

**Double-load**. A **double-load instruction** before any **instruction** ... troduced (because of **spill/reload instructions**), and the number of ...  
[compilers.cs.ucla.edu/ralf/publications/ralf-tech-report.pdf](http://compilers.cs.ucla.edu/ralf/publications/ralf-tech-report.pdf) - [Similar pages](#)